

IN THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 8, as follows.

A1
Processors often use a cache to improve performance and decrease system costs. Caches temporarily store recently accessed information (blocks of instructions or data) in a small memory that is faster to access than a larger main memory. Caches are effective because a block that has been accessed once is likely to be accessed soon again or is often near a recently accessed block. Thus, as a task executes, the working set of a task (the instructions and data currently required for the task) is stored in the cache in the event that the information may be accessed again. A cache typically maps multiple blocks of information from the main memory into one place in a cache, typically referred to as a "set." A "block" refers to the minimum unit of information that can be present in a cache and a "frame" is the place in a cache where a single block may be stored. In a set associative cache, multiple frames are grouped into sets. For example, as a two-way set associative cache has two frames in each set.

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Please amend the paragraph beginning at page 2, line 5, as follows.

A2
Generally, a method and apparatus are disclosed for allocating a section of a cache memory to one or more tasks. For example, one or more secondary tasks may be allocated a certain section of the cache, preserving the unallocated section of the cache for a primary task. The present invention transforms a set index value that identifies a corresponding set in the cache memory to a mapped set index value that constrains a given task to the corresponding allocated section of the cache. The allocated cache section of the cache can be varied by selecting an appropriate map function. When the map function is embodied as a logical and function, for example, individual sets can be included in an allocated section, for example, by setting a corresponding bit value to a binary value of one.

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Please amend the paragraph beginning at page 3, line 10, as follows.

A3
FIG. 1 illustrates a cache allocation system 100 in accordance with the present invention. As shown in FIG. 1, the cache allocation system 100 allocates a section 140 of the cache 150 to one or more tasks. For example, one or more secondary

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A3 tasks may be allocated a certain section of the cache. Thus, the secondary tasks may use only the allocated section of the cache, preserving the unallocated section for the primary task and consequently reducing the eviction of ~~lines~~ live lines of the primary task. In this manner, the number of misses suffered on resumption of the primary task is reduced. It is
5 recognized that limiting the cache space used by the secondary task may increase the misses for the secondary task. Thus, the benefits of the present invention are fully realized only in cases where the penalty on the secondary task is less than that experienced by the primary task due to eviction of lines accessed later. The benefit is
10 most evident in the case where the secondary task is sequential and large relative to the cache. The cache allocation system 100 and cache 150 can be part of a digital signal processor (DSP), microcontroller, microprocessor, application specific integrated circuit (ASIC) or another integrated circuit.
